

Application No: 10/027,911

PATENT

**REMARKS/ARGUMENTS**

Original claims 1-29 have been rejected by the Office. The elements of original claims 1, 2 and 3 have been combined to form amended claim 2. Original claims 1, 5 and 6 have been canceled. Claims 29-32 have been added. Claims 2-4 and 7-32 are pending in the present application.

Rejections Under 35 U.S.C. § 112

The Office has indicated that the claimed conductance of less than 0.5 mbos, recited in claims 5 and 6, has not been enabled. While one skilled in the art would readily implement the claimed limitation, reference to this limitation has been removed from the claim set of the application in the interest of furthering prosecution. Claims 5 and 6 have been canceled.

The Office has further indicated that there is no enablement for a trigger voltage of less than 10 volts. One of ordinary skill in the art of designing devices of the type recited in the claimed invention would readily understand how to implement such a feature. This is further supported by Li, cited by the Office at column 4, lines 58-64, which states how to implement such a voltage. Claims 1-17, 19, 27, and 28 either recite this limitation or depend from a claim that recites this limitation.

The Office has also indicated that the claimed capacitance of less than 120 femtofarads is not enabled, as recited or depended upon in claims 4-5. One skilled in the art of the claimed subject matter will appreciate that that removal of the resistors illustrated in prior art FIG. 1, i.e. removing the n-well and p-well ties, as illustrated in FIG. 5 of the application, enables the claimed capacitance to one skilled in the art.

For the reasons put forth above, the rejections put forth under 35 U.S.C. § 112 should be withdrawn.

Application No: 10/027,911

PATENT

35 U.S.C. § 102 and § 103 Rejections

Claim 2 has been amended to be an independent claim reciting elements of original claim 1. Amended claim 2 was rejected as original claim 2 under § 102 and § 103 as anticipated or obvious over Li. The Applicant Respectfully disagrees.

Claim 2 recites a first conductivity type junction formed between a first region of a first conductivity type and a second region of a second conductivity type; a second conductivity type junction formed between the second region and a third region of the first conductivity type; a third conductivity type junction formed between the third region and a fourth region of the second conductivity type, wherein the first, second and third conductivity type junctions are associated with a thyristor; and a low voltage trigger control coupled to the second region and the third region to provide a thyristor triggering current at a voltage of less than 10 volts; a first voltage reference node coupled to the first conductivity type junction; a second voltage reference node adapted to be isolated from the first voltage reference node during normal operating conditions, coupled to the fourth conductivity type junction to provide a current path between the first voltage reference node and the second voltage reference node during an electrostatic event, wherein the first voltage reference node and the second voltage reference node are to provide a common voltage reference.

Li does not disclose a first voltage reference node coupled to the first conductivity type junction and a second voltage reference node coupled to the forth conductivity type junction as recited. Therefore, because the recited element is not disclosed by Li, withdrawal of the rejection of claim 2 under § 102 is respectfully requested. Furthermore, unlike the recited invention of claim 2, Li does not suggest a first voltage reference node or a second voltage reference node as recited. Because Li does not disclose nor suggest these elements, and because Li provides no motivation absent the present application to include the recited elements, the present application is non-obvious and not anticipated. Withdrawal of the rejection of amended independent claim 2 under § 103 with respect to Li is respectfully requested.

 $V_R, V_C$

**Application No: 10/027,911**

**PATENT**

Amended claim 2 was rejected in the Office Action as original claim 2 under § 102 and § 103 as anticipated or obvious over Consiglio. The Applicant respectfully disagrees.

Consiglio does not disclose a first voltage reference node coupled to the first conductivity type junction and a second voltage reference node coupled to the forth conductivity type junction as recited. In fact, the apparatus of Consiglio explicitly discloses one of the two conductivity type junctions being connected to an I/O device and pad, as opposed to a voltage reference node. Therefore, because the recited element is not disclosed by Consiglio, withdrawal of the rejection of claim 2 under § 102 is respectfully requested. Furthermore, unlike the recited invention of claim 2, Consiglio does not suggest a first voltage reference node or a second voltage reference node. Because Consiglio does not disclose nor suggest these elements, and because Consiglio provides no motivation, absent the present application, to include a first and second voltage reference node as recited, withdrawal of the rejection of claim 2 under § 103 is respectfully requested.

Amended claim 2 was rejected as original claim 2 under § 102 and § 103 as anticipated or obvious over Avery. The Applicant Respectfully disagrees.

Avery does not disclose or suggest the first voltage reference node and the second voltage reference node as providing a common voltage reference as recited. Because Avery does not disclose the recited elements, and because Avery provides no motivation absent the present application, to include a first and second voltage reference node as recited, withdrawal of the rejection of claim 2 under § 103 is respectfully requested.

Amended claim 2 was rejected as original claim 2 under § 103 as anticipated or obvious over Li with Duvvury. The Applicant Respectfully disagrees.

In addition to the limitations of Li previously discussed, Duvvury does not disclose a first voltage reference node coupled to the first conductivity type junction and a second voltage

Application No: 10/027,911

PATENT

reference node coupled to the forth conductivity type junction as recited. Therefore, unlike the recited invention of claim 2, neither Li nor Duvvury disclose or suggest, alone or in combination, a first voltage reference node or a second voltage reference node as recited. Because neither Li nor Duvvury, disclose or suggest these elements, and because neither Li nor Duvvury provide motivation to implement the recited elements absent the present application, withdrawal of the rejection of amended claim 2 under § 103 is respectfully requested.

Claim 18 has been rejected by the Office under § 102 and §103 by the references previously cited. Claim 18 recites a thyristor formed in an integrated data processing device, the thyristor comprising a first conductivity type junction formed between a first region of a first conductivity type and a second region of a second conductivity type; a second conductivity type junction formed between the second region and a third region of the first conductivity type; a third conductivity type junction formed between the third region and a fourth region of the second conductivity type; and an anode node connected to one or more regions including the first region, wherein each of the one or more regions connected to the anode node are of a common connectivity type.

None of the references cited by the Office disclose an anode connected to one or more regions where each of the one or more regions connected to the anode are of a common connectivity type. For example, Li disclosed an anode coupled to two regions 136 and 132, however, the regions 126 and 132 are not of a common conductivity type as recited. Because none of the references disclose, or suggest, alone or in combination, the recited invention of claim 18, withdrawal of the rejections of claim 18 are respectfully requested.

Claim 21 has been rejected by the Office under § 102 and §103 by the references previously cited. Claim 21 recites an apparatus comprising a first voltage reference node to provide a first voltage reference; a second voltage reference node, adapted to be isolated from the first voltage reference node during normal operating conditions, to provide the first voltage reference; a thyristor coupled between the first voltage reference node and the second voltage

Application No: 10/027,911

PATENT

reference node to provide a current path between the first voltage reference node and the second voltage reference node during an electrostatic event.

None of these references disclose a first and second voltage reference node that are isolated, and that both provide the first voltage reference as recited. Because none of the references disclose, or suggest, alone or in combination, the recited invention of claim 21, withdrawal of the rejections of claim 21 are respectfully requested.

Claim 27 has been rejected by the Office under § 102 and §103 by the references previously cited. Claim 27 recites a method comprising detecting a voltage difference between a first voltage reference node and a second voltage reference node to determine when an electrostatic discharge event is occurring, wherein the first and second voltage reference are isolated from each other and are to provide the same voltage; providing conductive path through a thyristor when the voltage difference is less than approximately 10 volts.

None of the references disclose or suggest a first and second voltage where the first and second voltage reference are isolated from each other and provide the same voltage, as recited.

For the reasons put for above, each of the independent claims are believed in condition for allowance. Likewise, each of the dependent claims is in condition for allowance. In addition, the dependent claims provide additional points of novelty. For example, claim 3 recites that the first and second voltage reference nodes are both ground reference nodes.

In conclusion, Applicant has overcome all of the Office's rejections, and early notice of allowance to this effect is earnestly solicited. If, for any reason, the Office is unable to allow the Application on the next Office Action, and believes a telephone interview would be helpful, the Examiner is respectfully requested to contact the undersigned attorney.


Application No: 10/027,911

PATENT

Please charge additional fees relating to this matter, if any, to Toler, Larson & Abel  
deposit account number 50-2469.

Respectfully submitted,

7-14-03  
Date

  
J. Gustav Larson, Reg. No. 39,263  
Attorney for Applicant(s)  
TOLER, LARSON & ABEL, L.L.P.  
P.O. Box 29567  
Austin, Texas 78755-9567  
(512) 327-5515 (phone)  
(512) 327-5452 (fax)